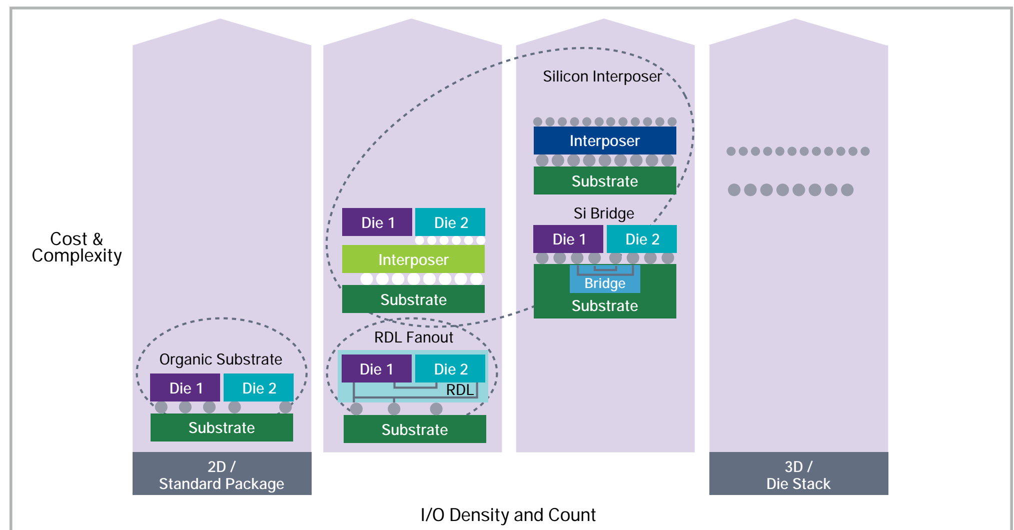
Motivation for Multi-Die Designs

A multi-die semiconductor device is one in which multiple homogeneous or heterogeneous dies are contained within a single package. Multi-die technology has been available for select uses for years, but it is gaining broader adoption in a wide variety of end applications, including high-performance computing, artificial intelligence (AI), automotive, and mobile. There are two main factors driving the increased deployment of this technology.

The first trend is the disaggregation of large monolithic system-on-chip (SoC) devices into smaller dies (also referred to as chiplets). This trend is partly driven by technological factors, such as when large chips approach the reticle limits of semiconductor manufacturing equipment. Even when manufacturing a large monolithic die is feasible, yield may be limited such that it becomes more economical to fabricate multiple smaller dies. Disaggregation might apply to large central processing units (CPUs), graphics processing units (GPUs), or AI accelerators in application domains such as data centers, automotive, mobile, gaming, etc.

The second (counter) trend is aggregation, with the integration into one package of a set of discrete ICs previously sharing a printed circuit board (PCB). The die-to-die communication in a multi-die chip consumes much less power and provides significantly higher throughput compared to chip-to-chip communication over a PCB. Multi-die integration is common in the networking domain, combining digital chips and co-packaged optics.



The Synopsys Multi-Die Test Solution

Multi-die designs are more costly to build and test than traditional single-die packages. Only one failed die in a multi-die configuration can cause the entire system to fail. Thus, the quality of each die and the integrity of the interconnect is critical. Experiencing late-stage failures can be catastrophic if not resolved quickly. Any effective solution mandates the use of a co-design platform, backed by several techniques and established standards. Figure 3 shows the key elements in the Synopsys multi-die test, monitor, and repair solution.

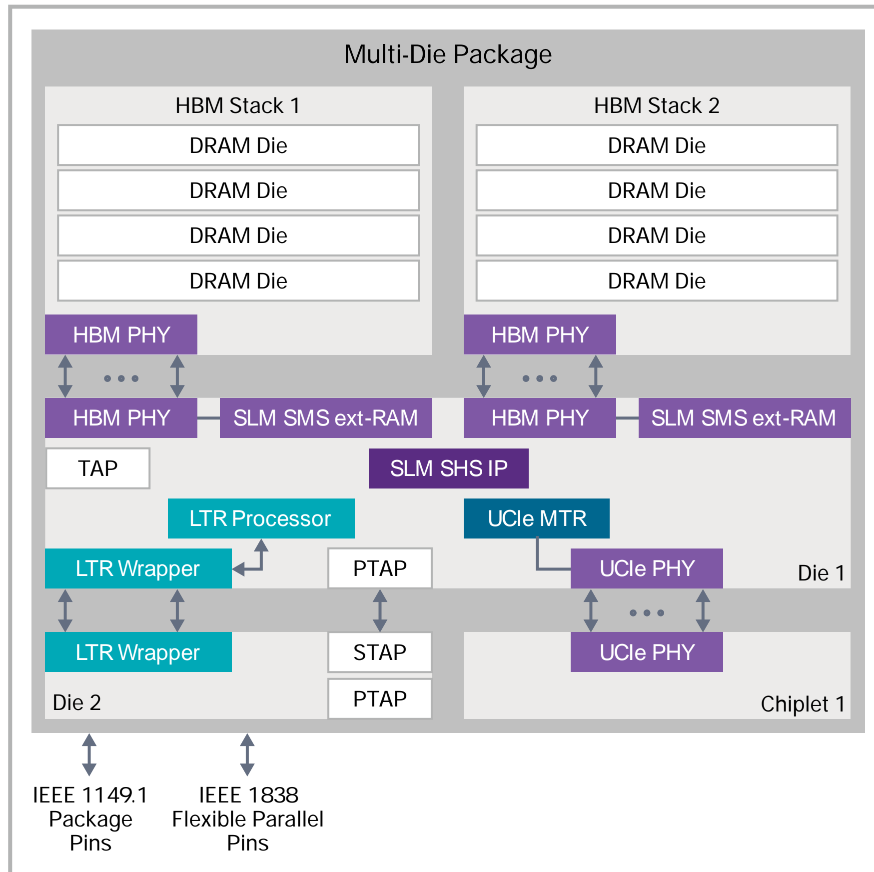


Figure 3: Elements of a multi-die test solution

The Synopsys solution for multi-die testability can handle all types of die-to-die interfaces:

- Logic-to-logic interfaces
  - Non-PHY based interfaces
    - Regular/low speed I/O based interfaces
    - High speed/high volume interfaces that feature redundancy
  - High speed PHY-to-PHY based interfaces such as UCIe
- High speed logic-to-memory interfaces such as HBM

For manufacturing, all aspects of intra-die, inter-die, and package level testing can be accomplished during the pre-bond, mid-bond and post-bonding stages. Synopsys offers a DFx solution that includes automated design for test (DFT) insertion with die-to-die and stack level access, die-to-die interconnect pattern generation with identification of faults, pattern porting for die-to-die and stack level, multi-die diagnosis and traceability as well as monitoring in-system for purposes such as predictive maintenance.

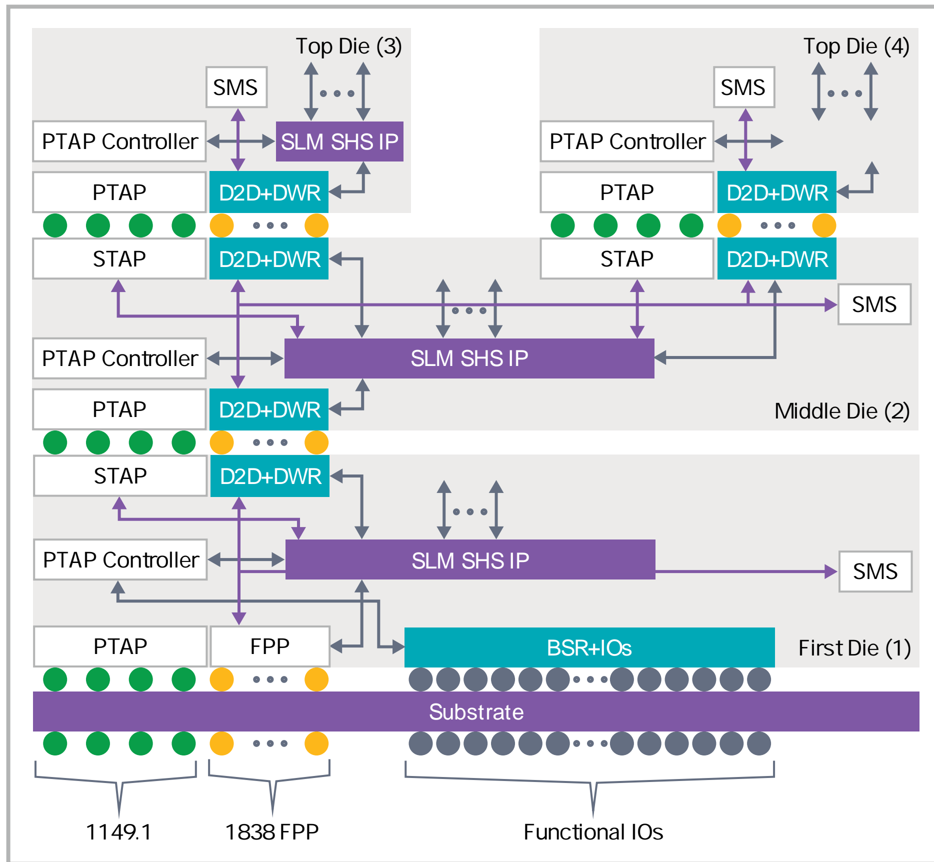
Synopsys Silicon Lifecycle Management (SLM) solution provides testability to cover all phases of the design: in-design, in-ramp, in-production, and in-field.

Synopsys Solutions for IEEE1838 and Lane Test and Repair (LTR)

The IEEE 1838 Standard for [illegible] provides the key DFT access architecture. This standard supports test of both individual dies and die-to-die interconnects. It is intended for low speed/low volume lanes.

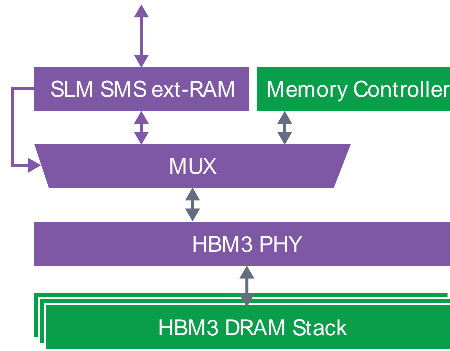
IEEE 1838 is a die-centric standard, applying to a die that is intended to be part of a multi-die design and defining die-level features. When compliant dies are combined into a stacked configuration, these features form a stack-level architecture for test of both intra-die circuitry and inter-die connections. It supports individual dies, partial stacks, and complete stacks, thus spanning pre-packaging, post-packaging, and board-level stages. Interconnects supported include through-silicon vias (TSVs), wire bonding, and other technologies.

Figure 4 presents a high-level view of the IEEE 1838 DFT architecture applied to a multi-die design. It includes the use of the Synopsys SLM SHS IP automated hierarchical test solution.



- Secondary Test Access Port (STAP)
  – IEEE 1149.1 port to interface with next/subsequent die
- Die Wrapper Register (DWR)
  – Die-to-die interconnect test between PHYs

Figure 6 shows how the Synopsys SLM SMS ext-RAM IP interconnects with the memory controller, the memory PHY, and the memory stack, using the HBM3 standard.



Summary

The growing importance of multi-die designs highlights the challenges associated with monitoring, testing and repair of packaged parts. Traditional probe-based methods cannot meet the demands. A solution must not only meet these challenges, but also span the full silicon lifecycle. Required DFx features must include test and repair of different types of die-to-die interfaces, perform lane test and repair, test for and diagnose known-good stack and known-good die, support extensive BIST capabilities, and offer in-field interconnect monitoring for purposes such as predictive maintenance. Synopsys provides a comprehensive and scalable solution for multi-die monitor, test, and repair.

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06/05/24.SNPS1366433529-Multi-Die-WP.

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